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TOPICAL REVIEW

Nonlinear properties of ballistic nanoelectronic devices

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Abstract

Advanced lithographic techniques allow the fabrication of strongly confined semiconductor nanostructures in which carriers travel without suffering from inelastic scattering even for bias voltages between the contacts exceeding several 100 mV. In the ballistic nonlinear transport regime, nanoelectronic devices show several electric properties very different from those of diffusive conductors. In this review we focus on recent studies of quantum wire transistors and Y-branch switches realized by electron beam lithography and wet etching of modulation doped GaAs/AlGaAs heterostructures in relation to nanoelectronic applications, such as a quantum wire amplifier, a compact AND gate based on a single Y-branch, feedback coupled bistable switching devices, static memory elements and a novel NAND gate with defined outputs realized by monolithically integrated Y-branches.

Contents

1. Introduction

The probability that charge carriers can travel in an electronic device without suffering collisions of any kind, i.e. ballistically, increases with the reduction of dimensionality [1, 2]. Pioneering work on transport in semiconductors had demonstrated effects which could be attributed to ballistic electron transport over a few μm [3–6]. In the past few decades, fabrication technologies have reached such a level that ballistic transport is entering the realm

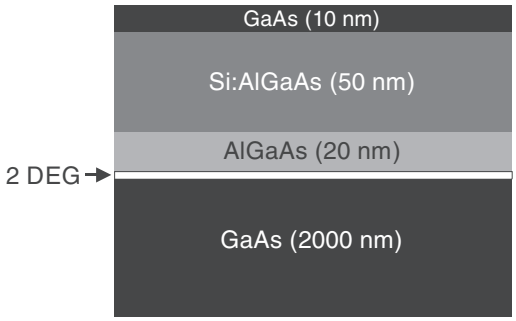

Figure 1. Schematic representation of the upper layers of a modulation doped GaAs/AlGaAs heterostructure. A two-dimensional electrons gas (2DEG) well separated by an undoped AlGaAs spacer from ionized donors forms at the AlGaAs/GaAs interface. A mean free path of electrons in the 2DEG exceeding 10 μm can be observed at cryogenic temperatures.

of the semiconductor industry as the scaling-down of transistors predicted by Moore's law will bring to the market integrated circuits containing billions of single nanoelectronic devices, each with a channel length shorter than the electron mean free path. Nowadays it is possible to realize artificially low dimensional structures in a controlled manner in a wide variety of different material systems with specific physical properties, very different from those of bulk semiconductors [7, 8] in which electrons can move freely in all three directions.

Two-dimensional electron systems are characterized by a strong confinement of the charged particles in one direction, on a length scale of the order of the de Broglie wavelength $\lambda = h/p$ with h the Planck constant and p the momentum. In the framework of transport physics two-dimensional electron gases are of special interest; these are formed e.g. at the inversion layer of a metal–oxide–semiconductor field effect transistor (MOSFET) or at the interface of a modulation doped semiconductor [9, 10]. Modulation doped semiconductor heterostructures also called high electron mobility transistors (HEMTs) are often the basis of low dimensional transport structures. High quality HEMTs can be realized for instance by molecular beam epitaxy (MBE) [11–13]. In the present study we present recent experiments on low dimensional channels formed in GaAs/AlGaAs HEMTs. A schematic cross section of the upper layers in a typical GaAs/AlGaAs HEMT is shown in figure 1. On a semi-insulating GaAs substrate a 2 μm thick undoped GaAs buffer was grown, followed by a 20 nm thick $Ga_{0.2}Al_{0.8}As$ spacer. Then doping with Si was performed during growth of 50 nm $Ga_{0.2}Al_{0.8}As$, which was finally capped by a 10 nm thick GaAs layer. In such a structure a two-dimensional electron gas (2DEG) is strongly confined in the direction of growth in an approximately triangle shaped potential formed at the heterointerface between the AlGaAs and the GaAs [14]. In addition to a high quality interface it is the local separation of ionized donors and the 2DEG by about 20 nm which results in long free mean paths of the electrons in the 2DEG due to a suppression of Coulomb scattering. In the direction of growth, i subbands exist with quantized energies E_i^z, occupied by electrons according to their energy. The Fermi energy, defined as the electrochemical potential of electrons at zero temperature, is typically of the order of $E_F \approx 10$ meV. In a 2DEG at cryogenic temperatures only the first subband is occupied with $E_F > E_1^z$.

2. Device fabrication

We used electron beam lithography with 100 kV acceleration voltage to define narrow channels in the 2DEG with widths down to a few tens of nm [15–17]. After a mask is defined into the

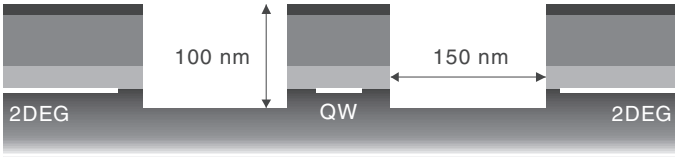

Figure 2. Schematic cross section of a side gate controlled quantum wire. The side gates are formed by the unconstrained 2DEG and are electrically isolated from the electrons in the quantum wire (QW). The electron density in the QW can be controlled by the side gates depending on the voltage difference between the 2DEG and the QW.

resists spun on top of the GaAs/AlGaAs HEMT, the sample is developed and a thin Al (∼13 nm) layer is evaporated. After a lift-off process all unexposed areas are removed. The Al structures serve as an efficient and robust mask for wet chemical etching. As depicted in figure 2 the upper layers of the GaAs/AlGaAs HEMT are removed down through the 2DEG. The etched trenches are approximately 100 nm deep and define both the quantum wires and wider adjacent regions used as self-aligned side gates.

Typically, such quantum wires are pinched off for zero gate voltage if the geometrical width of the quantum wire is smaller than 300 nm. However, sweeping up the side gate voltage the quantum wire is getting conductive above a positive threshold voltage. Above the threshold, with increasing gate voltage the electrical width of the wire increases. By means of magnetic depopulation the electrical width of quantum wires can be determined [18, 19]. It has been found that the maximal electrical width of quantum wires associated with the open state of the quantum wire is 20–40 nm smaller than the geometrical width of the quantum wire indicating that a dead layer of about 10–20 nm on each side exists in these wet etched GaAs/AlGaAs structures. The quantum wires can be efficiently controlled by the side gates and pinched off with channel resistances larger than several tens of GΩ. Due to the strong lateral confinement in the quantum wire, one-dimensional subbands exist with energies E_i of the ith subband and a density of states

$$D_{1D}(E) = \frac{g_s g_v}{2\pi\, h} \sum_i \sqrt{\frac{m^*}{2(E - E_i)}}\Theta(E - E_i) \tag{1}$$

with g_s and g_v the spin and valley degeneracy, respectively, m^* the effective mass and Θ the step function. In the linear regime, the response of a system scales linearly with the amplitude of the excitation. For transport properties of low dimensional structures, the linear regime is found for bias voltages much smaller than E_i/e and kT/e with kT the thermal energy. It is well known that at cryogenic temperatures the discrete character of the one-dimensional subbands in quantum wires is reflected in the quantization of the conductance in integer multiples of $G_0 = 2e^2/h$. This effect is characteristic for ballistic transport and was observed first for quantum point contacts [20, 21].

In the lower left part of figure 3(b) a configuration of a one-dimensional (1D) channel coupled adiabatically to two electron (2D) reservoirs each in thermal equilibrium is sketched. The electrochemical potentials are μ_d and μ_s. Upper left in figure 3 the corresponding energies are sketched together with the dispersion relation of the 1D channel for the k_x momentum component. A voltage difference V applied between the source and the drain results in a difference of the electrochemical potentials $\mu_s - \mu_d = eV$, which in turn generates a net current flow. For low temperatures and N occupied subbands in the 1D channel the current

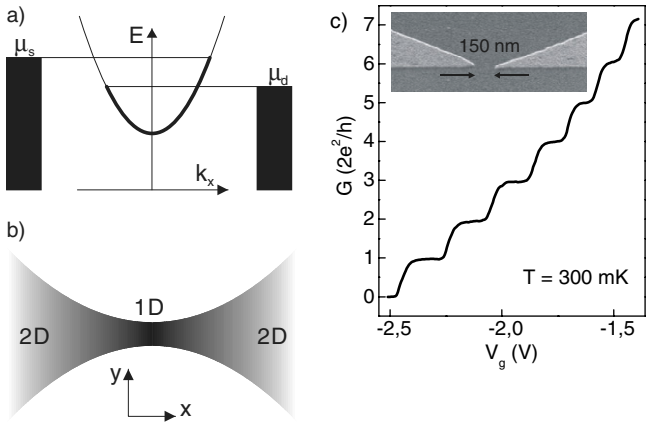

Figure 3. (a) Schematic representation of the dispersion relation of the lowest subband of a one-dimensional channel coupled to two wide electron reservoirs with different electrochemical potentials μ_d and μ_s. In the lower part (b) the corresponding geometry is shown. (c) Conductance of a quantum point contact as a function of the gate voltage conducted at a temperature of 300 mK. The inset shows an electron microscope image of the split gate structure with a 150 nm wide slit.

can be described by [22]

$$I_{1D} = e \sum_{n=1}^{N} \int_{\mu_d}^{\mu_{d+eV}} D_{1D}(E)\, v_x(E) T_n(E)\, dE. \tag{2}$$

Possible scattering events are considered by the transmission coefficient $T_n(E)$, which is associated with the probability that an electron with energy E in mode n is transmitted through the 1D channel. The group velocity $v_x = \frac{1}{\hbar}\frac{dE}{dk_x}$ is proportional to the slope of the dispersion curve $E(k_x)$, which is indirectly proportional to the density of states. Thus the physical origin of the conductance steps is related to the fact that in 1D the product $D_{1D}(E)v_x(E) = g_s g_v/h$ is constant. In the ballistic regime $T_n(E) \equiv 1$ and the conductance $G = I/V = \sum_1^N G_n = N \times \frac{2e^2}{h} = N \times G_0$, in which each occupied subband contributes $G_n = G_0 = \frac{2e^2}{h}$.

In the right part of figure 3 quantized conductance observed for a split gate defined quantum point contact at a temperature of 300 mK is shown. The quantum point contact corresponds to a 1D constriction in a 2DEG, which is defined by narrow gate electrodes on top of a GaAs based HEMT structure illustrated in the electron microscope image in the inset to figure 3(c). Negative gate voltages applied to the split gates with respect to the drain reservoir deplete the 2DEG below the gates. Below a critical gate voltage electrons are transmitted only through the 1D channel directly below the split gate opening. At even lower gate voltages 1D subbands are depopulated one at a time with decreasing gate voltage and thus the conductance decreases in a step-like manner. Quantized conductance observed in the linear regime of nanoelectronic devices can be interpreted as a signature of ballistic electron transport. However, the 1D subband spacings in a split gate defined structure are limited to of the order of a few meV. In addition, applying critical large bias voltages, electron transport beneath the depletion gates sets in, hampering the study of nonlinear transport properties in nanoelectronic devices. For this purpose wet etched structures like quantum wires and Y-branched junctions are appropriated due to their large subband energies and the robust lateral confinement. All studies reported in the following have been conducted by immersing the structures in liquid He at a temperature of 4.2 K.

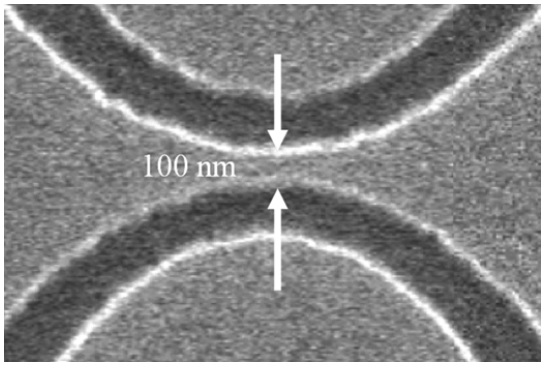

Figure 4. Electron microscope image of a planar quantum wire transistor. The 100 nm wide quantum wire is isolated from the two side gates by 200 nm wide and 90 nm deep trenches.

3. Studies of quantum wire transistors in the nonlinear transport regime

By the beginning of the 1980s it had become possible to realize electrically conductive quantum wires with a strong lateral confinement in two dimensions [23, 24]. Since that time quantum wires have been studied in many cases as regards their electrical and optical properties [25–30]. Recently, it has become possible that excellent one-dimensional conductors often referred to as nanotubes could be fabricated exploiting self-organization techniques on the basis of e.g. carbon and silicon [31–37]. As regards electrical properties and particularly with regard to ballistic transport, gate controlled quantum wires are of special interest [38–44]. Quantum wire transistors can be controlled efficiently either via planar side gates or via top gates [45–49].

The topic of the following section is related to the transport properties of quantum wire transistors, which are controlled by side gates. The transistors are based on modulation doped GaAs/AlGaAs heterostructures and have been fabricated by electron beam lithography and wet chemical etching. An electron microscope image (top view) of a side gate controlled quantum wire transistor is shown in figure 4. The quantum wire has a geometrical width of 100 nm at the site of the constriction and widens into bullhorn-like electron reservoirs serving as the source contact and drain contacts. In the regions of the 200 nm wide and 90 nm deep trenches the upper layers of the heterostructure have been removed down through the 2DEG. Consequently the isolated side gates are capacitively coupled to the quantum wire.

First, the quantum wire transistor was studied in the linear and weak nonlinear transport regimes. For this purpose the set-up sketched in figure 5 was used. A sine-like excitation voltage V_{exc} with an amplitude of 70 μV and a frequency of 77 Hz was applied to the drain contact of the quantum wire. For measurements in the nonlinear regime a direct current (dc) voltage could be easily superimposed to the alternating current (ac) signal. This type of measurement mode is often referred to as transport spectroscopy. The drain current has been directly detected via the current input of a lock-in amplifier. In order to overcome the contact resistance, the voltage drop across the quantum wire has been detected directly via two additional voltage probes. Due to the chosen four-probe set-up the differential conductance G of the quantum wire is then defined as the ratio of the lock-in detected drain current and the voltage across the sample. At first, the differential conductance G of the quantum wire was determined for the linear transport regime as a function of the gate voltage.

The differential conductance G of the quantum wire was determined for the linear transport regime as a function of the gate voltage. Figure 6(a) shows the dependence of G together with the derivative $\mathrm{d}G/\mathrm{d}V_{\mathrm{g}}$ versus the gate voltage. The quantum wire is highly resistive for gate voltages smaller than 75 mV, i.e. the first subband is energetically above the electrochemical

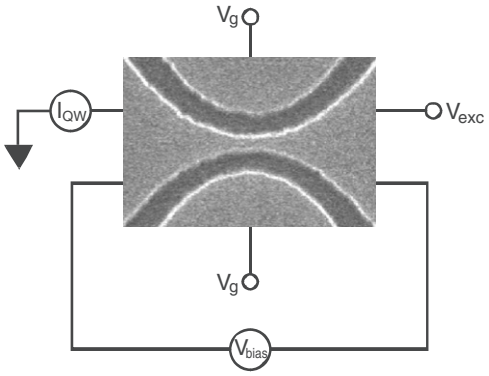

Figure 5. Schematic representation of the transport spectroscopy set-up. A gate voltage V_g is applied to the side gates. A sine-like excitation voltage V_{exc}, which can have a dc voltage superimposed is applied between the source and the drain of the quantum wire. The left contact is used as the common ground. The differential conductance $G = \frac{dI_{QW}}{dV_{bias}}$ is determined as the ratio of the current I_{QW} and the bias voltage V_{bias}, using a four-probe lock-in technique.

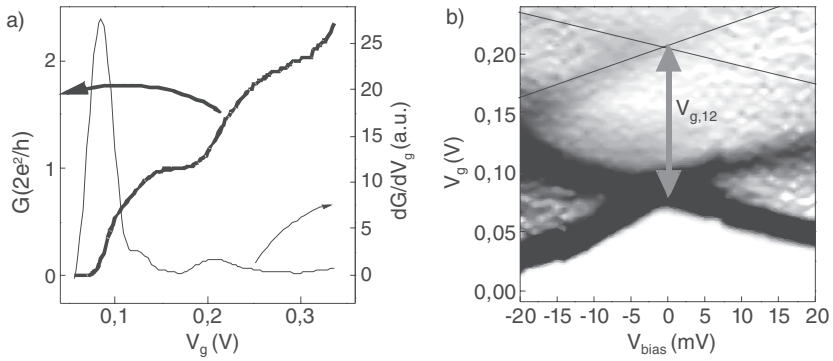

Figure 6. (a) Gate voltage dependence of the differential conductance G of a side gate controlled quantum wire as well as dG/dV_g, the corresponding derivative with respect to the gate voltage. (b) Greyscale plot of the dG/dV_g as a function of the bias voltage V_{bias} and V_g.

potential both in the source and the drain reservoirs. For gate voltages larger than 75 mV G increases with increasing gate voltage. The further curvature forms a step in the conductance with $dG/dV_g = 0$. At $V_g = 0.18$ V the population of the second subband starts and a second step in the conductance can be observed at $V_g \approx 0.30$ V. An interesting feature in the $G(V_g)$ trace is the structure at $G = 0.7 \times \frac{2e^2}{h}$, which in particular clearly appears in dG/dV_g. The 0.7 structure is believed to be associated with a spin polarization of the 1D electron gas [50–53].

In order to analyse quantitatively the energetic separation of the 1D subbands in the quantum wire, transport spectroscopy can be used [47, 54, 55]. For this reason a dc voltage V_{bias} ranging between −20 and 20 mV was superimposed on the ac signal and the differential conductance G was measured as a function of the gate voltage and the bias voltage. The derivative dG/dV_g is shown in a greyscale presentation in the right part of figure 6. The regions corresponding to small (large) change of G for a small gate voltage sweep are depicted as bright (dark) contrast. With respect to $V_{bias} = 0$, a peak splitting with increasing bias voltage of the dG/dV_g maxima at $V_{g1} = 0.085$ V and $V_{g2} = 0.208$ V can be observed.

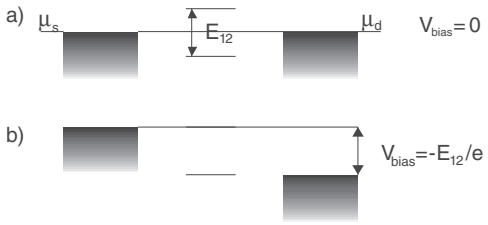

Figure 7. Illustration of the electrochemical potentials in the source reservoir and the drain reservoir and the first two subbands with an energy separation of E_{12} in a quantum wire transistor for (a) vanishing bias voltage and (b) $V_{\mathrm{bias}} = -E_{12}/e$.

The splitting of the $\mathrm{d}G/\mathrm{d}V_{\mathrm{g}}$ maxima in the weak nonlinear regime is ascribed to a finite bias voltage on the energies of the 1D subbands relative to the electrochemical potentials μ_{s} and μ_{d} of the source reservoir and the drain reservoirs, respectively [56]. As illustrated in figure 7 the electrochemical potential of the source equals the electrochemical potential of the drain for $V_{\mathrm{bias}} = 0$. In contrast, finite bias voltages result in a shift of the electrochemical potentials as well as the subbands. In the latter case it is the drain field in the channel which lowers the barrier by $\Delta E_{\mathrm{sub}} = -\sigma e \Delta V_{\mathrm{bias}}$. This lowering is a principal effect in short channel devices and known as drain induced barrier lowering (DIBL). For symmetrical devices and small bias voltages, $\sigma = 1/2$ [1]. An increase of V_{bias} leads to the situation shown in figure 7(b), for which the second subband aligns with the electrochemical potential of the source, which in turn leads to an increase of $\mathrm{d}G/\mathrm{d}V_{\mathrm{g}}$. $V_{\mathrm{bias},12} = -E_{12}/e$ is exactly the voltage for which the regions of maximal $\mathrm{d}G/\mathrm{d}V_{\mathrm{g}}$ cross each other emerging from discrete $\mathrm{d}G/\mathrm{d}V_{\mathrm{g}}$ peaks at $V_{\mathrm{bias}} = 0$. The energy separation between the first and the second subband is thus $eV_{\mathrm{bias},12}$, the voltage at which the thin black and the thick black lines presented in figure 6(b) would cross each other. From an extrapolation (not shown) $E_{12} \approx 27$ meV is determined. Subband energies of the order of 20 meV have been found in wet etched GaAs/AlGaAs quantum wires reflecting a strong lateral confinement [57, 58]. It addition, the subband separation can now be used to extract the gate efficiency η, a measure of the leverage factor determining how a gate sweep changes the conduction band barrier in the channel. For the present quantum wire the difference of the gate voltages $V_{\mathrm{g},12} = V_{\mathrm{g}2} - V_{\mathrm{g}1} = 0.123$ V (see figure 6(b)). Thus $\eta = E_{12}/(eV_{\mathrm{g},12}) \sim 0.2$.

Comparable to the function of a field effect transistor (FET) is the working principle of a side gate controlled quantum wire transistor, as the conductance of the channel is significantly controlled via the capacitively coupled gates [59, 60]. However, in contrast to the case for an FET in a quantum wire transistor, charge transport is not carried via a two-dimensional conductive layer but takes place in a nanostructured one-dimensional channel. In order to study the amplification characteristics of a nanoelectronic quantum wire we have chosen a source circuit layout, i.e. the source is connected to ground and the bias voltage V_{bias} is applied in series with an $R_{\mathrm{d}} = 500\ \mathrm{k}\Omega$ resistor to the drain as shown in figure 8 by a corresponding circuit diagram. In this configuration the dependence of the voltage V_{d} at the drain contact on the gate voltage applied to the side gates was studied for a temperature $T = 4.2$ K, by immersing the sample into liquid helium.

The transfer characteristic is shown in figure 9 for $V_{\mathrm{bias}} = 1$ V. For gate voltages of $V_{\mathrm{g}} < 20$ mV the output voltage V_{d} is equal to the bias voltage, i.e. the quantum wire is highly resistive. With increasing gate voltage $V_{\mathrm{g}} > 0$ a current flow through the quantum wire sets in and therefore the output voltage decreases until saturation is reached with $V_{\mathrm{d}} \approx 70$ mV. The inverted character of the transfer curve is accompanied by a differential voltage gain $g = \frac{\mathrm{d}V_{\mathrm{d}}}{\mathrm{d}V_{\mathrm{g}}}$.

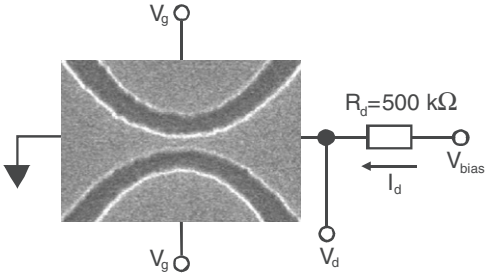

Figure 8. Schematic representation of the circuit used to study the amplification characteristics of a quantum wire transistor.

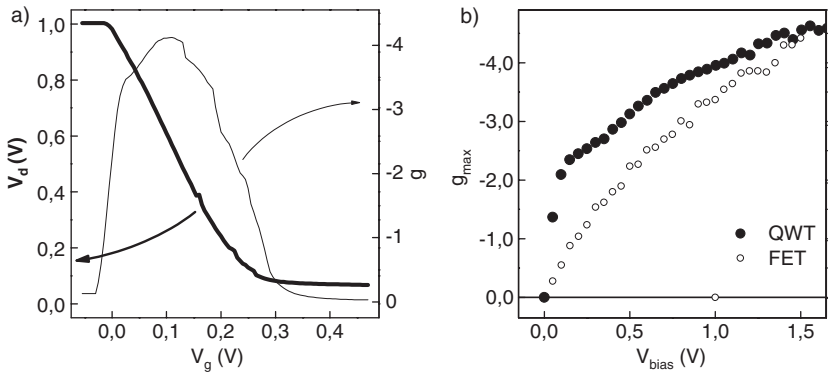

Figure 9. (a) Transfer characteristic $V_d(V_g)$ and amplification dependence $g(V_g)$ of a quantum wire transistor (QWT) for $V_{bias} = 1$ V and a temperature $T = 4$ K. (b) The maximum of the differential voltage gain g_{max} of a QWT and an n-type channel field effect transistor (FET) as a function of the bias voltage.

The dependence of $g(V_g)$ is plotted in the right part of figure 9. Evidently the differential voltage gain depends sensitively on the input voltage with a maximum $g_{max} = -4.1$ at $V_g = 0.11$ V.

In order to study the amplification with respect to the bias voltage we have recorded several transfer characteristics in the range $0 \leqslant V_{bias} \leqslant 1.5$ V with $\Delta V_{bias} = 50$ mV. The voltage–voltage traces have been numerically differentiated and the resulting $g_{MAX}(V_g)$ dependence is shown in the right part of figure 9. There are several interesting aspects which should be mentioned. First, even for bias voltage as small as 50 mV the differential voltage gain is larger than unity. Second the gain increases with increasing bias voltage strongly until it forms a step-like curvature at $V_{bias} = 0.15$ V. We made an interesting observation by analysing the step height at the centre for $V_{bias} = 0.25$ V. At this bias voltage $g_{max} = -2.5$, and thus the maximum transconductance is $-g_{MAX}/R = 2.5/500\,000$ A V^{-1}. Later we will show that the effective gate voltage change $\Delta V_g \times \eta$, i.e. the gate voltage change multiplied by the gate leverage factor, is $0.13\Delta V_g$ for $V_{bias} = 0.25$ V. Thus the effective transconductance corresponding to the step observed in figure 9(b) is $2.5/(0.13 \times 500\,000)\ A/V \approx \frac{e^2}{h}$. Although this value represents a rough estimate, we conclude that for the quantum wire studied the transconductance shows a plateau at $\frac{e^2}{h} \times \eta$. Possibly this step-like feature in the $g_{max}(V_{bias})$ trace can be interpreted as a signature of ballistic transport in the nonlinear transport regime. Interestingly a second modulation appears at about $V_{bias} = 0.7$ V. However, then the gain starts to saturate with a maximum value of -4.6 at $V_{bias} = 1.5$ V. In the framework of a 1D finite

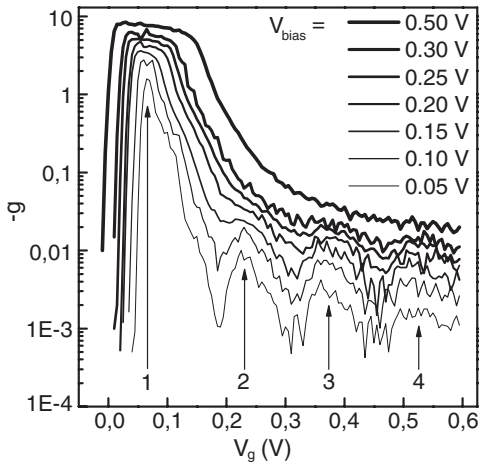

Figure 10. Amplification characteristic of a quantum wire transistor on a logarithmic scale. The curves related to bias voltages 0.10, 0.15, 0.20 V . . . have been multiplied by factors 1.25, 1.5, 1.75, . . ., respectively.

harmonic potential model according to the observed subband spacing one can conclude that the wire has an effective electrical width of 25 nm [61]. Thus the maximum transconductance is $\mathrm{d}I_\mathrm{d}/\mathrm{d}V_\mathrm{g} = (1/R)\,\mathrm{d}V_\mathrm{d}/\mathrm{d}V_\mathrm{g} = 341\ \mu\mathrm{S}\,\mu\mathrm{m}^{-1}$. For the purpose of achieving a better comparison we have modelled the transfer characteristics of a standard n-type channel MOSFET according to [62] with a drain resistance 100 Ω, and likewise for different bias voltages, and extracted g_max numerically. These results are presented together with experimental data obtained for the quantum wire transistor versus the bias voltage in the right part of figure 9. Also for the FET g_max increases with the bias voltage; however, in contrast to the case for the quantum wire, for the FET g_max increases with an approximately constant curvature. For the quantum wire the gain increases almost abruptly for small bias voltages until a bias voltage of about 150 mV is reached.

So as to qualify this observation, the transfer characteristics and respectively the differential voltage gain in the range for small bias voltages have been analysed. In particular, a logarithmic presentation of $-g(V_\mathrm{g})$ is found to be informative for bias voltage $V_\mathrm{bias} \leqslant 0.5$ V. In producing this, the curves have been offset vertically for clarity by factors of 1.25, 1.50, 1.75,... with respect to the bottom trace. On inspection of figure 10, one can clearly identify nonlinearities at $V_\mathrm{g} = 0.065$, 0.23, 0.37 and 0.53 V, at which local maxima exist in the amplification characteristic. While the voltage positions of the maxima remain nearly constant it is the characteristic shape of the peaks labelled as 2, 3 and 4 which decrease significantly with increasing bias voltage. The maximum labelled as 1 in figure 10 persists up to a bias voltage of 0.5 V; however a broadening of the amplification peak takes place with increasing bias.

If we compare the peaks in the gain dependence with the right part of figure 6, it seems reasonable to suggest that the oscillations in $g(V_\mathrm{g})$ are associated with the successive occupation one 1D subbands. Thus, the oscillations are interpreted as a signature of ballistic transport of electrons through the wire in the strongly nonlinear regime. Both $\mathrm{d}G/\mathrm{d}V_\mathrm{g}$ and $\mathrm{d}V_\mathrm{d}/\mathrm{d}V_\mathrm{g}$ show a pronounced maximum close to the threshold of the quantum wire transistor followed by another maximum and in particular even several subsequent maxima are evident in the $\mathrm{d}V_\mathrm{d}/\mathrm{d}V_\mathrm{g}$ trace, and the gate voltage separation between the maxima in both experiments is about 100 mV.

Of particular interest are the subthreshold characteristics of transistors especially in relation to digital applications, as the subthreshold describes the transition from the highly

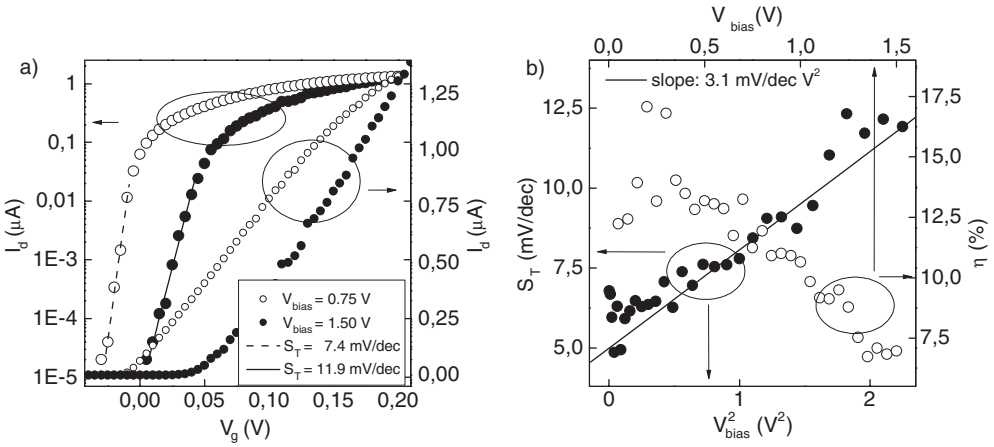

Figure 11. (a) Drain current of a quantum wire transistor as a function of the gate voltage presented both on a logarithmic and on a linear scale for bias voltages $V_{\rm bias} = 0.75$ and 1.50 V. (b) Dependence of the subthreshold swing $S_{\rm T}$ and the gate efficiency η on the bias voltage $V_{\rm bias}$.

resistive OFF state to the conductive ON state [63]. An important parameter in the subthreshold regime is the subthreshold swing, which is the gate voltage swing required to change the drain current by one decade. As regards a reduction of the power loss in a transistor it is desired that the subthreshold swing $S_{\rm T}$ should be as small as possible. At a temperature T, the drain current in the subthreshold regime is described by

$$I_{\rm d} \propto \exp\left(\frac{e\eta\left(V_{\rm g} - V_{\rm T}\right)}{k\,T}\right), \tag{3}$$

with the threshold voltage $V_{\rm T}$. The factor η describes the gate efficiency. For a perfect gate structure the gate leverage factor $\eta = 1$. Using equation (3), it is possible to extract the theoretical lower bound of the subthreshold swing which is $S_{\rm lim} = \ln(10)kT/e$, approximately 60 mV at room temperature. Indeed, $S_{\rm lim}$ has been observed for Si based quantum wire transistors with diameters of only 5 nm [64–67]. The gate efficiency is a measure of how the potential profile along the channel is affected by the gate voltage. For decreasing temperatures, $S_{\rm T}$ should decrease; however tunnelling currents between the source and the drain, particularly for short channel transistors, limit the observation of very small subthreshold swings [68].

Exploiting equation (3), the subthreshold characteristic of the side gate controlled quantum wire can be estimated directly from a logarithmic presentation of the drain current as a function of the gate voltage. Therefore the drain current $I_{\rm d}$ was extracted from the $V_{\rm d}(V_{\rm g})$ characteristics. Example curves for bias voltages $V_{\rm bias} = 0.75$ and 1.50 V are shown in figure 11(a). At first $\log(I_{\rm d})$ increases linearly from $I_{\rm d} \approx 1.0 \times 10^{-5}$ μA up to $I_{\rm d} \approx 1.0 \times 10^{-2}$ μA. Above a gate voltage of approximately 0 and 65 mV for $V_{\rm bias} = 0.75$ and 1.50 V, respectively, the transistor reaches the channel threshold and a pronounced current flow sets in, which is clearly reflected in the corresponding linear scale representation. The subthreshold swing can be estimated from a linear fit of the $\log(I_{\rm d}(V_{\rm g}))$ trace below the threshold and the following values are found: $S_{\rm T} = 7.4$ mV dec^{-1} ($V_{\rm bias} = 0.75$ V) and $S_{\rm T} = 11.9$ mV dec^{-1} ($V_{\rm bias} = 1.50$ V), from which a gate efficiency $\eta < 1$ can be concluded.

We extracted $S_{\rm T}$ from the experimental data for $0.050\ {\rm V} \leqslant V_{\rm bias} \leqslant 1.50\ {\rm V}$ and analysed a functional dependence between $S_{\rm T}$ and $V_{\rm bias}$. It has been found that a parabolic dependence between $S_{\rm T}$ and $V_{\rm bias}$ fits well, which the plot of $S_{\rm T}$ versus $V^2_{\rm bias}$ in the right part of figure 11

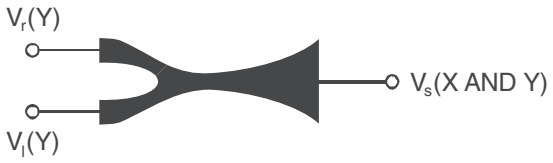

Figure 12. Schematic representation of a ballistic Y-branch exploited as an AND gate with the input voltages V_l and V_r as well as the output voltage V_s. All voltages refer to a common ground.

reflects nicely. The subthreshold swing increases in a quadratic manner of approximately 5 mV dec^{-1} for $V_\mathrm{bias} = 0.1$ V up to 12 mV dec^{-1} for $V_\mathrm{bias} = 1.5$ V. A fitting of the data point gives a proportional constant of 3.1 mV dec^{-1} V^{-2}. Neglecting tunnelling currents, the gate efficiency η can be calculated directly from equation (3) via the subthreshold swing with $\eta = S_\mathrm{T}/S_\mathrm{lim}$. That has been done for the experimental values of S and the result is shown in the figure 11(b). It can be clearly seen that the gate efficiency decreases from $\eta = 0.15$ for $V_\mathrm{bias} < 0.5$ V with increasing bias voltage and finally at $V_\mathrm{bias} = 1.5$ V a value of $\eta = 0.07$ is reached. Although the gate efficiencies of $\eta = 0.15$ extracted from this experiment for bias voltages up to 0.5 V are smaller than the values found for the analysis of the transport spectroscopy described above, the results verify our interpretations, as tunnelling currents which have not been considered would lead to larger subthreshold swings and thus smaller values of η.

4. Nonlinear transport in electron Y-branches: ballistic rectifier and logic AND gate

In many respects the transport characteristics of ballistic structures differ from those of conventional electronic devices. In contrast to the case for diffusive conductors, in which carriers reach thermal equilibrium at a length scale far below the dimensions of the conductor, in ballistic devices charges traverse the channel conserving the electrochemical potential of the originating contacts. Consequently no electrical resistance should be detectable inside a ballistic conductor due to the absence of inelastic scattering. The non-local resistance of a ballistic device is created in the contact regions, where a large number of modes discharge into a few modes of a one-dimensional conductor. Recently, this effect was nicely demonstrated exploiting cleverly designed contacts as well as gate structures on high quality quantum wires [69].

Likewise, a nanoelectronic junction of three quantum wires with an extension of the branching section much smaller than the mean free path of electrons represents a ballistic conductor, and thus its electrical characteristics should be different from those of a geometrically similar, but diffusive, three-terminal conductor. Indeed, in nanometric Y-branches a rectification effect can be observed, which is not obvious in macroscopic diffusive systems. The ballistic rectification can be exploited for the realization of extremely compact logic gates and circuits. As an example, in the following discussion an AND gate is explained.

The Y-shaped junction shown schematically in figure 12 allows an investigation of the ballistic rectification effect. In particular, the Y-branch junction studied has a mirror symmetry with respect to the axis along one branch, hereafter referred to as the 'stem'; i.e. the device is identical with respect to a permutation of the other branches. If the geometrical symmetry of the Y-branch is reflected in all electrical properties, it is clear that in a currentless measurement one should observe at the stem a voltage drop described by the arithmetic mean of the voltages applied to the branches. Indeed, that is the result that one observes by studying a junction

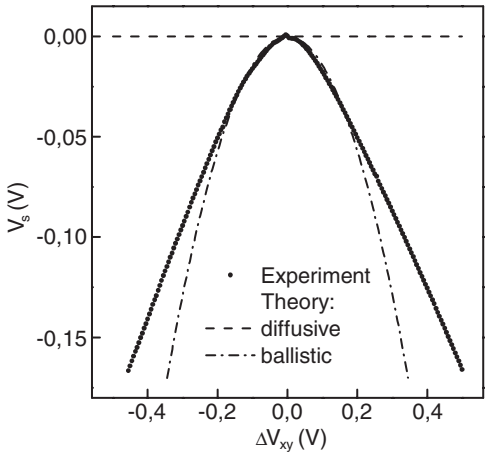

Figure 13. The stem voltage V_s of a Y-junction as a function of the branch voltage difference $\Delta V_{xy} = V_x - V_y$ varied in push–pull mode at $T = 4.2$ K. The experimental curve for $|\Delta V_{xy}| < 75$ mV was fitted according to equation (5) with the parameter $\xi = 12.1\ \mathrm{V}^{-1}$.

operated in the diffusive linear transport regime. If Ohm's law is a valid approach for the description of the current voltage, such a junction corresponds to a star-like circuit of three equal constant resistors. According to Ohm's law if the voltages at the branches are varied in push–pull mode with $V_l = -V_r$, the voltage at the stem will be $V_s = 0$.

In contrast, for a nanoelectronic junction in which electrons pass ballistically through the branching section, although the device is geometrically symmetric an electric asymmetry is introduced. Hence, the measured voltage at the stem tends more to the negative voltage [70, 71]. Figure 13 demonstrates this rectification effect, reflected in the stem voltage behaviour for voltage sweeps of $\Delta V_{xy} = V_x - V_y$ at the 100 nm wide branches of a Y-junction. The voltage at the stem V_s was detected with a high impedance voltmeter and thus the current through the stem $I_s \sim 0$, while V_x and V_y were varied in a push–pull-like manner with $V_x + V_y = 0$. For the trivial case $\Delta V_{xy} = 0$ ($V_x = V_y = 0$), $V_s = 0$, as expected classically. However, for finite voltage difference $\Delta V_{xy} \neq 0$ the stem voltage V_s tends to the more negative branch voltage whereas the deviation from the classical value increases with ΔV_{xy}.

The high structural quality of the junction investigated is reflected in the nearly perfect symmetry of the experimental $V_s(\Delta V_{xy})$ characteristic with $V_s(\Delta V_{xy}) \sim V_s(-\Delta V_{xy})$. The observed rectification, i.e. $V_s < (V_x + V_y)/2$, for all $\Delta V_{xy} \neq 0$ can be explained by the ballistic nature of electron transport in the nanometric three-terminal junction. For clarity, the energies of electrons moving along the channel connecting the reservoir of the left branch with the reservoir of the right branch are depicted schematically. For voltages at the branches with $V_l > V_r$, effectively electrons are injected from the right branch with an electrochemical potential μ_r into the junction and the voltage V_s, i.e. the electrochemical potential μ_s at the stem reservoir, is measured without a net current flow through the stem. In the case of diffusive transport (figure 14(a)), multiple inelastic scattering occurs along the channel, which in turn reduces the kinetic energy of the electrons. Thus the detectable electrochemical potential in the stem is clearly smaller than μ_r and equals $(\mu_r + \mu_l)/2$ for a symmetric Y-junction. However, for ballistic or even quasi-ballistic transport, a different scenario can be drawn, as reflected in figure 14(b). In the ballistic regime inelastic scattering of the injected electrons along the relevant channel can be neglected and is almost of no relevance in the quasi-ballistic regime. The electrons essentially conserve their initial electrochemical potential by passing through

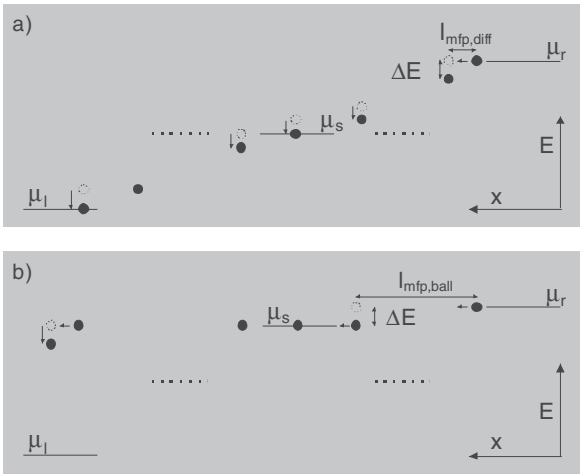

Figure 14. Schematic energy diagram for ballistic and quasi-ballistic rectification. (a) Diffusive transport: the electron mean free path $l_{\mathrm{mfp,diff}}$ is much shorter than the active channel length between the reservoirs of the left and right branches. (b) Quasi-ballistic transport: the electron mean free path $l_{\mathrm{mfp,ball}}$ is of the order of the channel length.

the junction. In the left reservoir, the injected electrons reach thermal equilibrium on a length scale which is correlated with the mean free path of the unconstrained 2DEG. Ideally, at the stem one can detect an electron energy $\mu_{\mathrm{s}} = \mu_{\mathrm{r}}$. However, in practice this energy is only approximately reached due to partial inelastic scatterings of the quasi-ballistic electrons.

Qualitatively, ballistic rectification can be described by an ansatz based on the Landauer–Büttiker formalism [72–75]. In this model, the three-terminal junction is described as a ballistic cavity which is adiabatically coupled to the three electron reservoirs via quantum point contacts. For each of the quantum point contacts, a specific transmission coefficient T_{ij} and reflection coefficients R_{ij} are associated with $i, j = \mathrm{l}, \mathrm{r}$ and s. The current through the stem can then be described by

$$I_{\mathrm{s}} = \frac{2e}{h}\left[\int [N_{\mathrm{s}}(E) - R_{\mathrm{ss}}(E)] f\,(E-\mu_{\mathrm{s}}, T)\,\mathrm{d}E - \sum_{i=\mathrm{l,r}} \int T_{si}(E) f(E-\mu_i, T)\,\mathrm{d}E\right], \quad (4)$$

with N_{s} the occupied subbands in the stem, $\mu_{\mathrm{l}} = \mu_{\mathrm{F}} - eV$ the electrochemical potential in the left reservoir and $\mu_{\mathrm{r}} = \mu_{\mathrm{F}} - eV$ the electrochemical potential in the right reservoir. μ_{F} is the electrochemical potential of the reservoirs for negligibly small bias voltages. The Fermi–Dirac function $f(E-\mu_i, T)$ describes the occupation probability of the states in reservoir i with the energy $E-\mu_i$ and the temperature T. Finally, the voltage at the stem can be calculated from equation (4) with $V_{\mathrm{s}} = -\mu_{\mathrm{s}}/e$ assuming $I_{\mathrm{s}} = 0$ (currentless measurement of V_{s}). Assuming that no reflections in the stem occur, the voltage V_{s} depends on the bias voltage V along the branches:

$$V_{\mathrm{s}} = \tfrac{1}{2}\xi V^2 + \sigma(V^4), \quad (5)$$

with the curvature $\xi = -e\frac{\partial T_{\mathrm{sl}}(\mu_{\mathrm{F}},T)/\partial\mu_{\mathrm{F}}}{T_{\mathrm{sl}}(\mu_{\mathrm{F}},T)}$.

The transmission coefficients $T_{\mathrm{sl}} = T_{\mathrm{ls}} = T_{\mathrm{sr}} = T_{\mathrm{rs}}$ are positive and thus a negative curvature for the V_{s} (V) characteristic is expected for the case where T_{sl} is an increasing function of the electrochemical potential μ_{F}. In the case of a linear dependence between T_{sl} and μ_{F} the curvature reduces to $\xi = -e/\mu_{\mathrm{F}}$, i.e. the curvature is reciprocally proportional to

X	Y	C = X AND Y
H	H	H
H	L	L
L	H	L
L	L	L

Figure 15. Truth table of an AND gate with the inputs X and Y and the output C.

the Fermi energy in the stem reservoir. Actually, the $V_s(\Delta V_{xy})$ characteristic shown in figure 13 in push–pull fashion for $|\Delta V_{xy}| < 75$ mV fits very well with a parabolic form using a fitting parameter $\xi = 12.1\ \mathrm{V}^{-1}$. For the further curve progression, i.e. $|\Delta V_{xy}| > 75$ mV, the deviation between the parabolic fit and the measured data increases. In this strongly nonlinear voltage regime these simple approximations of the model are not valid. For the strongly nonlinear regime several aspects such as increased energy relaxation, intervalley scattering and space charge have to be considered [76–78].

The presented nonlinear transport properties of ballistic Y-junctions lead to several interesting nanoelectronic applications. On the one hand, this Y-junction may serve as a frequency mixer or a coincidence counter; on the other hand, the functionality of an extremely compact AND gate has been demonstrated [71, 79, 80]. A logic AND gate with a truth table presented in figure 15 has the property that the output is in a logic H state only if both inputs are set as logic H states; else the output is in the L state. Interestingly, due to the ballistic rectification, a Y-shaped junction intrinsically fulfils the requirements of an AND gate. For an experimental demonstration, the stem voltage V_s of a nanoelectronic Y-branch was measured at $T = 4.2$ K for all input voltage combinations at the branches important for the verification of the AND truth. The corresponding experimental data are shown in figure 16. The input voltages V_x and V_y applied to the left and the right branch of the Y-branch are varied digitally between 0 and 0.5 V as can be seen in the low and middle parts of figure 16. A signal is referred to as logic H (L) for a voltage higher (lower) than $V_{sig} = 0.25$ V. Clearly, the output is only at H ($V_s > 0.25$ V) if H is at both inputs simultaneously. In particular, due to the ballistic rectification, V_s is low for $(XY) = (\mathrm{LH})$ ($V_s = 0$) or $(XY) = (\mathrm{HL})$ ($V_s = 0$), while for a symmetric Y-shaped junction in a diffusive transport regime the undefined state $V_s = 0.25$ V is expected.

5. Amplification properties and memory function of electron Y-branch switches in the nonlinear regime

The realization of nanoelectronic amplifiers is essential for the success of any concept of a future nanoelectronic paradigm. Here we present studies of Y-branches exploited as transistor elements. It has been found that a splitting of the channel leads to enhanced switching properties compared to single-quantum-wire transistors. This enhanced function is based on the working principle of side gated electron Y-branch switches (YBSs). A YBS offers the possibility of guiding electrons from the stem (source) into either of the branches (drain) via a lateral electric field. This mechanism is associated with a change of electron momentum rather than a change in electron energy and can be controlled by voltages applied to the lateral gates along the split

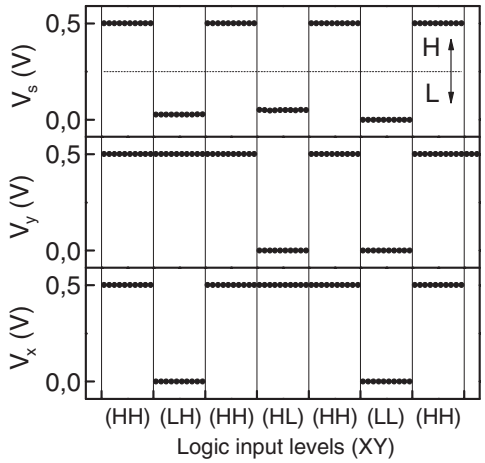

Figure 16. Demonstration of the AND functionality of a Y-shaped ballistic junction.

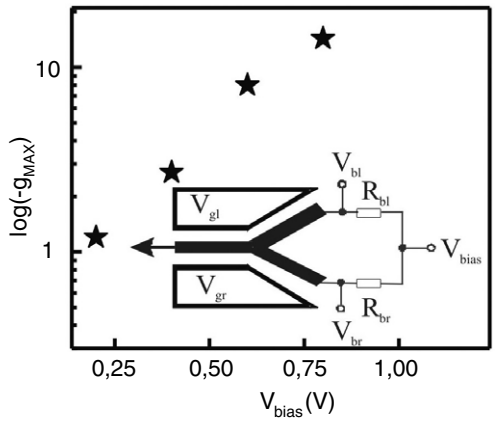

Figure 17. Maximum negative differential voltage gain $g_{\max}$ (log scale) as a function of the bias voltage V_{bias}. Inset: circuit diagram used to investigate the properties of a YBS used as a differential amplifier.

channel: e.g. a positive voltage at the left side gate leads to a larger electron current into the left branch. This effect can be exploited to drive a YBS as an efficient differential amplifier in such a way that voltage differences ΔV_{in} at the input stage are enhanced at the site of the output state with voltage difference $|\Delta V_{\text{out}}| > |\Delta V_{\text{in}}|$.

In the nonlinear transport regime any difference in the currents through the branches can be transformed into voltage differences between the branches using a set-up schematically shown as an inset in figure 17. Here, a bias voltage V_{bias} is applied in series with two resistors (R_{bl} and R_{br}) to the left and right branches of a YBS. The stem of the YBS is connected to ground.

Using the set-up depicted in figure 17 the YBS amplifies voltage differences $\Delta V_{\text{g}} = V_{\text{gl}} - V_{\text{gr}}$ into larger voltage differences $\Delta V_{\text{b}} = V_{\text{bl}} - V_{\text{br}}$ at the branches. Figure 18 shows ΔV_{b} as a function of ΔV_{g} for $V_{\text{bias}} = 0.8$ V. For negative values of ΔV_{g} electrons injected from the stem into the branching section are preferentially steered into the right branch, which in turn leads to a low voltage $V_{\text{br}} = V_{\text{bias}} - I_{\text{r}} R_{\text{br}}$ at the right branch with I_{r} the current in the right branch. On the other hand, a high voltage is detected at the left branch leading to $\Delta V_{\text{b}} > 0$ and $\Delta V_{\text{g}} < 0$. In particular, an amplification of the input voltage difference at the lateral gates is observed with $|\frac{\mathrm{d}\Delta V_{\text{b}}}{\mathrm{d}\Delta V_{\text{g}}}| > 1$. Similarly, positive voltage differences ΔV_{g} are amplified into negative voltage differences ΔV_{b} with $|\Delta V_{\text{b}}| > |\Delta V_{\text{g}}|$.

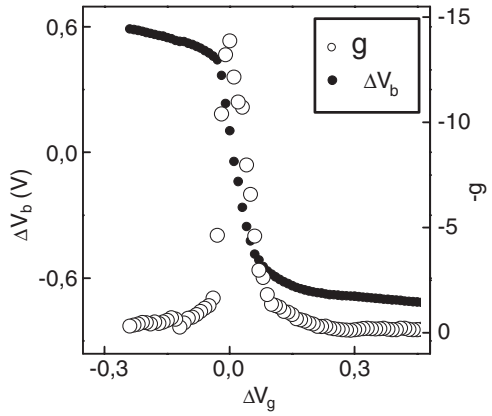

Figure 18. Output characteristic of a YBS based differential amplifier for $V_{\mathrm{bias}} = 0.8$ V. The output voltage difference ΔV_{b} between the branches and the differential voltage gain g are plotted versus the input voltage difference ΔV_{g} between the lateral gates.

A qualitative measure of the amplification is the differential voltage gain $g = \mathrm{d}(\Delta V_{\mathrm{b}})/\mathrm{d}(\Delta V_{\mathrm{g}})$ which is shown as a function of ΔV_{g} in figure 18. Evidently, the differential gain has a pronounced maximum with $g_{\max} = -14.3$ for $\Delta V_{\mathrm{g}} = 0$ where small changes of gate voltages affect the distribution of injected electrons into the left or right branch most efficiently. With increasing $|\Delta V_{\mathrm{g}}|$ the gain decreases strongly until saturation sets in.

The differential voltage gain depends strongly on the applied bias voltage which can be seen in figure 17, where $g_{\max}$ is plotted versus V_{bias}. For small bias voltages $g_{\max}$ increases linearly with V_{bias} and exceeds a value of one at $V_{\mathrm{bias}} = 0.2$ V. Above $V_{\mathrm{bias}} = 0.4$ V a superlinear increase of the maximum differential gain is observed leading to $g_{\max} = -15$. In this way the gain characteristic of a YBS differs significantly from that of a QWT for which $g_{\max}$ shows a negative curvature for increasing bias voltage (see figure 9). The superlinear $g_{\max}(V_{\mathrm{bias}})$ characteristic of the YBS is explained in terms of a self-gating mechanism due to a capacitive coupling of the branches. Not only do voltage differences at the branches control the split channel but also voltage differences between the branches themselves have an impact on the switching characteristics of a YBS in the nonlinear transport regime. In particular, due to a capacitive coupling of the branches a larger voltage at one branch opens the adjacent branch [81, 82]. Let us consider a Y-branch with load resistances connected to the branches. The stem is used as the common ground and positive identical voltages are applied to load resistances. A lateral field due to a bias voltage between the side gates leads to an enhanced negative current flow into the left branch, e.g. a positive voltage is applied to the left side gate and a negative one to the right side gate. Such an electric field will direct electrons from the stem more efficiently into the left branch. Because of the resistance a difference in current will create a difference of the voltage at the branches. In particular, the branch with the larger current has the lower voltage and the branch with the smaller current the higher voltage. Therefore, the branch with the larger current is gated more positively by the other branch, which further reduces the voltage at the branch. The branch with the lower current is in turn additionally depleted by the adjacent branch with the lower voltage, which further increases the voltage. The result is a bistability, where the current is directed to either of the branches.

Interestingly, by feeding back an output voltage at one branch to the adjacent side gate a YBS shows a bistable switching behaviour. A bistable switch is an ideal digital switch, for which the output voltage as a function of the input voltage is not continuously varied, but passes

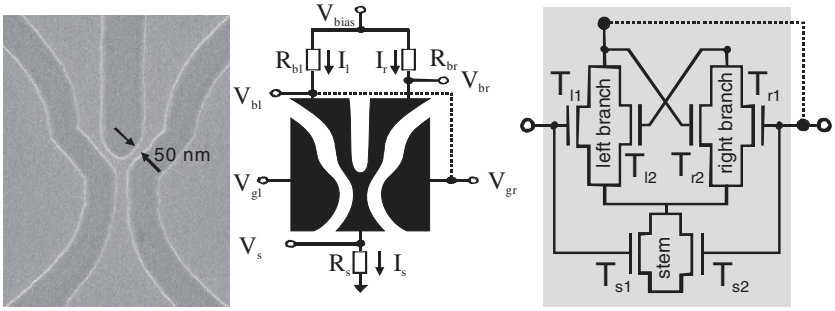

Figure 19. Scanning electron microscope image (left), measurement set-up (centre) and equivalent circuit diagram (right) of the YBS used as a Schmitt trigger device. The external feedback from the left branch to the right side gate enables bistable switching. The resistances are $R_{bl} = R_{br} = 10\ M\Omega$, $R_S = 100\ k\Omega$. V_{gl} serves as the input voltage and the voltage drops at the branches, V_{bl} and V_{br}, are the measured output voltages.

abruptly into two stable states referred to as the logic low state (L) or logic high state (H). The switching from L (H) to H (L) is triggered either by dc voltages applied at a static input or by signal pulses applied at a dynamic input. Both states are stable until the input exceeds a critical threshold voltage. To the family of such multivibrators belongs the Schmitt trigger [83]. The output signal of a Schmitt trigger stays in the L state as long as the input signal is smaller than the corresponding threshold voltage $V_{L\to H}$ and flips instantaneously to the H state when $V_{L\to H}$ is reached. The H state is stable until the input voltage undergoes the second threshold voltage $V_{H\to L} < V_{L\to H}$ and the output voltage switches back into the H state. Characteristically, a pronounced switching hysteresis $V_{Hys} = V_{L\to H} - V_{H\to L}$ occurs. Recently, the investigation of Schmitt triggers and bistable transitions has attracted considerable interest, theoretical as well as experimental [84–91]. Schmitt triggers are used in analogue and in particular digital integrated circuits in order to reduce noise and interfering signals. Therefore a Schmitt trigger is an important device in the output stage of logic circuits.

The measurement set-up for a nanoelectronic proposal of such a Schmitt trigger based on a single YBS is shown in the right part of figure 19. The bias voltage V_{bias} is applied at the branches in series with the external resistances $R_{bl,br} = 10\ M\Omega$, whereas the stem is connected to ground with a resistance $R_s = 100\ k\Omega$. The voltage at the left side gate serves as the input voltage. The feedback which is required for a bistable transition is achieved by an external coupling of the left branch reservoir with the right side gate.

Voltage dependences $V_{bl}(V_{gl})$ and $V_{br}(V_{gl})$ are shown in figure 20 for a bias voltage $V_{bias} = 2.0$ V. V_{gl} was swept between 0.426 and 0. 708 V. At $V_{gl} = 0.426$ V the conductance of the left branch is low, i.e. the current through the stem flows efficiently on the right branch ($I_r = 38$ nA). Thus the voltage at the left branch decreases as the current through the left branch increases with increasing gate voltage V_{gl}. In contrast, the voltage at the right branch rises slightly until the threshold voltage $V_{gl} = V_{L\to H} = 0.604$ V is reached. Thereby the logic states L and H are referred to the right branch serving as output. At this gate voltage the right branch voltage V_{br} switches from 0.216 to 2.0 V, while V_{bl} is reduced to 0.945 V. If the gate sweep direction is returned, the switching process is reversed at $V_{gl} = V_{H\to L} = 0.525$ V. The corresponding voltage hysteresis is about $V_{Hys} = 79$ mV. The resolution of the switching transition is about 1 μV.

As reported in [90] the origin for such a bistable transition is a capacitive interaction of the side gates due to a self-gating of the branches. Voltages which are applied at the side gates influence the electrical width in the stem as well as the width of the adjacent branch.

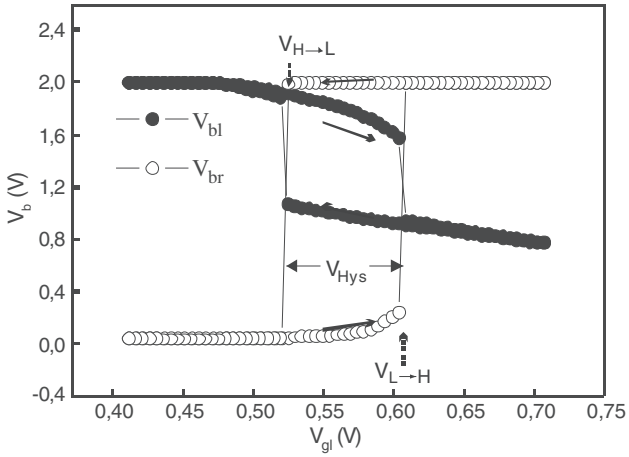

Figure 20. Typical result of the input characteristic for a bistable transition due to external feedback. The hysteretic loop is sketched for V_{bl} as well as for V_{br} as a function of V_{gr}.

Without an external coupling we have shown that the YBS acts as a differential amplifier with a maximal gain of about $g = |\Delta V_b/\Delta V_g| = 30$. An external coupling between the left branch and the right side gate enhances significantly the control of the channel conductance. With an equivalent circuit diagram depicted in the right part of figure 19 this effect can be explained in the following way: for $V_{gl} = 0.604$ V the transistors T_{r1}, T_{r2} and T_{s2} are pinched off. Hence, the whole bias voltage drops at the right channel, $V_{br} = V_{bias} = 2.0$ V ($I_r = 0$), and T_{l2} becomes conductive. A reduction of the voltage at the left side gate decreases the conductivity of the transistors T_{s1} and T_{l1}. Therefore V_{bl} increases, whereby V_{br} decreases due to a higher conductivity of T_{s2}, T_{r1} and T_{r2} triggered by V_{bl}. In this voltage range the behaviour of the circuit is reversible as long as the threshold $V_{H\to L} = 0.525$ V is not reached. However, starting at this voltage self-gating takes place and in addition the external feedback pinches off the left branch and opens the right branch abruptly. A further decrease of V_{gl} reduces the current I_l strongly. As a consequence the equivalent transistors T_{r1} and T_{s2} as well as (with a lower efficiency) T_{r2} open their channels resulting in an abrupt transition of V_{br} to the L state that pinches off T_{l2}. This again leads to an increase of V_{bl} due to the self-induced gating. The abrupt voltage transition can only be reversed for $V_{gl} > 0.525$ V, i.e. for $V_{gl} = V_{L\to H} = 0.604$ V.

These measurements in the nonlinear transport regime show that a YBS can serve as a compact switching element with the functionality of a Schmitt trigger. The interplay of an intrinsic coupling between the branches and an external feedback of one branch to the opposing side gate causes a feedback loop and enables a bistable switching.

As regards technical applications of bistable switching elements, short switching times in the range of nanoseconds are necessary in order to reduce the access time for the stored data. Therefore we have also studied dynamic features of the nanoelectronic Schmitt trigger in the following way. The measurement set-up is the same as the one used before with $V_{bias} = 2.0$ V, $R_{bl} = R_{br} = 10$ MΩ and $R_s = 100$ kΩ. The only difference to the previous investigation is that switching transitions are not triggered any longer by a continuous increase or decrease of a dc input voltage. They are activated by rectangle shaped pulses which are generated by a function generator. A static dc voltage at the left side gate is applied only in order to adjust a proper voltage offset. This voltage offset is used to prepare the state transition from L to H and is 5 mV lower than the threshold voltage $V_{L\to H}$. The pulse amplitude is 2.0 V and the pulse

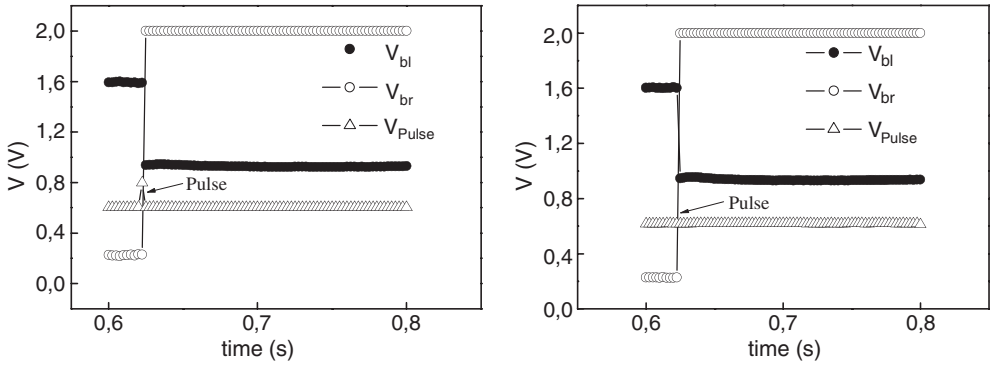

Figure 21. Switching behaviour for a rectangle shaped pulse with a pulse length of 50 ms (left part) and for 50 ns (right part). The switching behaviour is for the applied pulses not dependent on the pulse length.

width is lowered from 50 ms to 50 ns. The pulse width of 50 ns represents the lower limit of the present set-up.

Figure 21 shows the measurement results for a bistable transition from L to H for a pulse width of 50 ms and 50 ns, respectively. One can see the time dependent branch voltages V_{bl} and V_{br}. The voltage offset is 0.6 V and the corresponding threshold voltage is 0.604 V. At $t = 0.623$ s the pulse is set in both measurements. The 50 ms pulse can be identified in the left picture, whereas the 50 ns pulse cannot be resolved. By setting the pulse applied at the left side gate the conductivity of the left branch increases and V_{bl} drops from 1.589 to 0.936 V. According to the above-mentioned equivalent circuit diagram, T_{l1} and T_{s1} are coupled by the self-gating of the branches and the external feedback. Due to the resulting H state being stable and the offset voltage being above the threshold voltage $V_{\mathrm{H}\to\mathrm{L}}$, the high state is also maintained on the falling edge of the trigger pulse.

In particular, the number of electrons needed to trigger the internal and external feedback and hence the switching from L to H is of special interest. In order to estimate the number of these switching carriers let us assume that a rectangle shaped pulse applied at the left side gate influences only the current in the left branch. For an ideal case, with optimized self-induced switching and feedback, only a few carriers are required for triggering the bistable transition. An upper bound of the critical charge can be extracted from the current swing triggered by a short pulse presented in figure 22. On applying this pulse for a short time t_0, the electrical width of the left branch is increased. A current sets in and initiates internal and external feedback, which in turn increases additionally the electrical width of the left branch. The result is an abrupt current swing $I_{\mathrm{H}} = 0.0656\ \mu$V. Therefore, an upper limit of the switching charge $Q_{\max}$ is given by product of the current swing I_{H} and the corresponding pulse length t_0 of the applied pulse $Q_{\max} = \int_0^{t_0} I(t)\,\mathrm{d}t = I_{\mathrm{H}}\,t_0$. In the framework of this model the 50 ns pulse causes a switching charge not larger than 3.3×10^{-15} A s. This corresponds to an upper limit of approximately 20 500 electrons required for the current swing. In the right part of figure 22 the upper limit estimation is shown for pulse lengths ranging from 50 ms to 50 ns. The linear dependence was elongated down to smaller pulse lengths. However, this regime could actually not be acquired experimentally due to limitations of the set-up. In any way, according to our model for a pulse with $t_0 = 3$ ns only an amount of 1000 switching electrons are required.

Along with the investigation of new transistor concepts and miniaturized integrated circuit designs featuring high speed, low power consumption and dissipation, the storage of data in

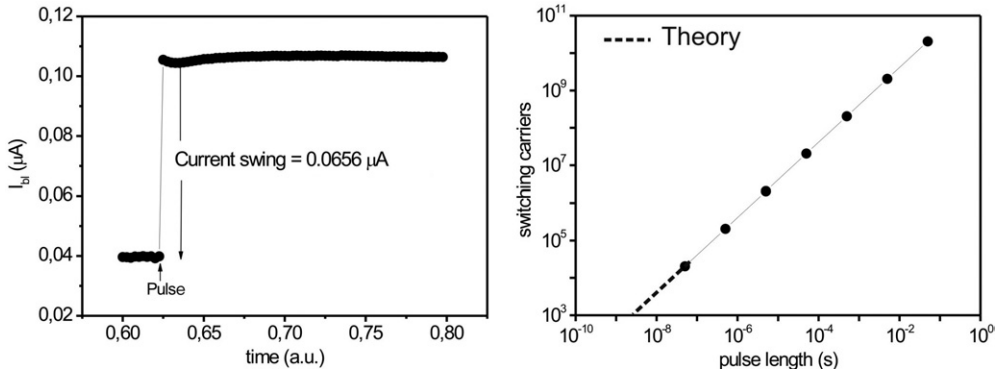

Figure 22. Left part: the current swing in the left branch for a pulse length of 50 ns. The current swing is about 0.0656 μA and remains almost constant for the whole interval of pulse length investigated, ranging between 50 ms and 50 ns. Right part: estimated number of electrons contributing to the switching in the left branch as a function of the pulse length.

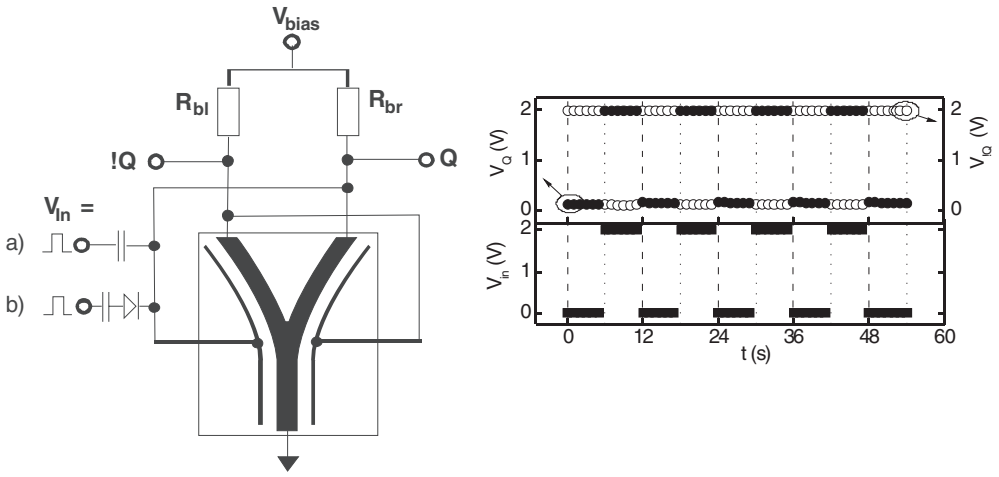

Figure 23. Left part: schematic view of the YBS used as a memory element. Configuration (a) represents a simple memory element enabled for writing by positive and negative trigger pulses. These trigger pulses evolve from differentiation of a rectangle shaped input pulse due to an external capacitor, $C = 68$ nF. Configuration (b) represents a simple monoflip. A rectifying diode is used in order to filter negative trigger pulses. Right part: corresponding response to negative and positive trigger pulses for configuration (a).

volatile and non-volatile memory cells represents a very active field of investigation [92–95]. Recently, a nanoelectronic SRAM device based on carbon nanotubes was presented [96]. Interestingly, a YBS can also be used as a static memory device [97]. For that purpose, each branch is connected to the opposing side gate, i.e. here we use two external feedback couplings.

In order to analyse the static memory effect we first tested the response of the doubly feedback connected YBS to signal pulses applied at the side gates used as dynamic input stages. The left part of figure 23 shows the corresponding measurement set-up. The bias voltage $V_{\rm bias} = 2.0$ V was applied in series with two resistances $R_{\rm bl} = R_{\rm br} = 10$ MΩ to the branches, whereas the stem is connected to ground. The feedback required for bistable switching is obtained when each branch reservoir is coupled to the opposing side gate. The

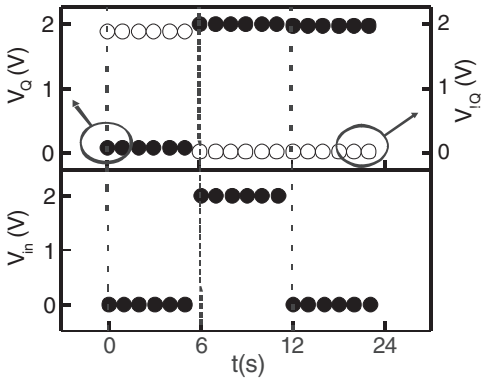

Figure 24. Demonstration of a simple monoflip based on configuration (b).

voltage drop at the left (right) channel is referred to !Q (Q). In configuration (a), a capacitor with a capacitance of 68 nF transforms applied rectangular pulses at the rising and falling edge into sharp positive and negative trigger pulses, whereas in (b), the negative trigger is filtered by the rectifying external diode.

The lower right part of figure 23 shows the time dependent input signal applied at the left side gate which can be identified as rectangle shaped pulses. The pulse height is about 2.0 V. At different times $t_{pos} = 6, 18, 30, 42$ s the rising edges of the rectangle shaped pulses appear, which are differentiated due to the capacitance to a positive trigger pulse (not shown), whereas at $t_{neg} = 12, 24, 36, 48$ s the falling edges of the rectangle shaped pulses are differentiated to negative trigger pulses. The resulting switching of the output voltages is presented in the upper right part of figure 23. !Q (Q) changes from H (L) to L (H) at the positive edge of the input (positive trigger pulse) signal and then back to !Q = H (Q = L) for the negative edge of the input signal (negative trigger pulse).

A positive trigger pulse increases as long as the trigger pulse is applied at the electrical width of the left branch, and as described above the internal and external feedback thus decreases the conductance in the right branch. After this positive trigger pulse the information Q = H and !Q = L is stored because the low voltage at the left branch and the corresponding low voltage at the right side gate keep the right branch at the H state and vice versa. In contrast a low trigger pulse decreases the electrical width of the left branch. As a consequence the conductance in the right branch increases and the states Q = L and !Q = H are stable because each branch and the corresponding opposing side gate stabilize the other branch.

In order to show that this memory effect can really be triggered by small trigger pulses the negative trigger pulses at the falling edge of the rectangle shaped pulses are now filtered by an external diode in configuration (b) of figure 23 (left). The result is presented in figure 24. Until the time $t = 11$ s the result is the same as in figure 23 (right). Indeed at $t = 12$ s, the result is different from figure 23, where at the falling edge of the input signal no back-switching occurs, i.e. one rectangle shaped pulse changed the output state from Q = L (!Q = H) to Q = H (!Q = L) and the result is stored by internal and external feedback. So configuration (b) represents a simple monoflip.

The ongoing miniaturization of microelectronic devices, initiated, beyond the investigation of new transistor concepts, the development of alternatives for the realization of static memory elements. Besides the above-described internal and external feedback mechanism exploited in the Schmitt trigger, a YBS has been demonstrated to serve as the active part of a static random access memory (SRAM) cell. In order to test the memory function a clock signal C is needed

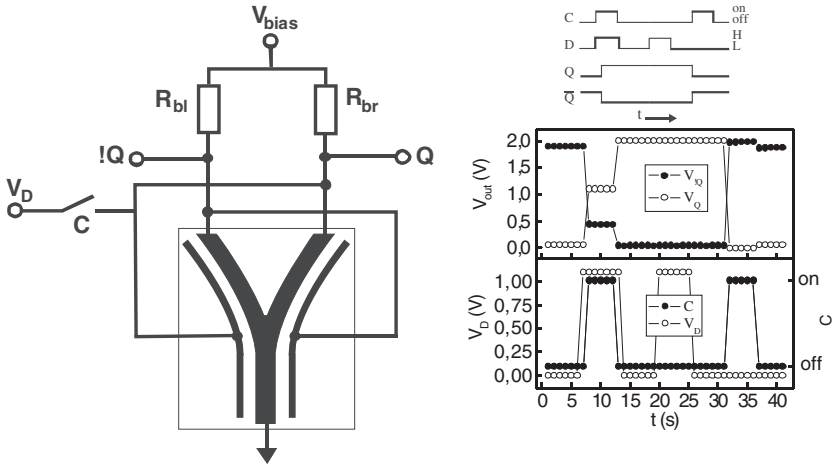

Figure 25. Left part: schematic circuit of a D-FlipFlop as the active part of an SRAM device. V_D is the corresponding data signal and C is the clock signal implemented by a relay. Right part: demonstration of a D-FlipFlop-like switching behaviour.

which connects or disconnects a data signal D to/from the left side gate (and right branch) of a YBS. We have realized such a clock signal by a relay which switches the data signal V_D on and off as one can see in the left part of figure 25. In the upper right part of figure 25 a scheme for a logic D-FlipFlop output, Q and !Q, for several important variations of logic inputs C and D is illustrated. It can be seen that only when the relay is closed (C = ON, W = H) is the memory element enabled for a new setting through a write pulse, so an applied signal V_D changes the states Q and !Q, e.g. for C = ON and D = H the resulting state is Q = H and !Q = L, whereas for C = ON and D = L the switching results in Q = L and !Q = H. The stored information is maintained when the relay is switched off (C = OFF, W = L).

In view of the realization of novel logic devices the NAND gate plays an important role, because all complex logic operations can be built up from interconnected NAND gates [62]. Logic circuitry based on Y-branch switches has been proposed and theoretically analysed by Palm *et al* [98]. As already demonstrated, a ballistic Y-branch fulfils intrinsically the logic AND function. In addition, a YBS can also be exploited as an amplifier and, in particular, as a nanoelectronic Schmitt trigger with the advantage of generating well defined output levels. Here we demonstrate that a monolithic integration of a YBS AND gate in conjunction with as YBS Schmitt trigger leads to a compact AND/NAND gate with excellent electrical characteristics.

It is clear that the continuous and linear switching characteristic of a single YBS is inappropriate for achieving well defined logic levels. Therefore the connection of the YBS stem to a side gate of a second YBS not only enables the inversion of the AND function, but also amplifies the input signal. By using in addition an external YBS Schmitt trigger feedback for the second YBS, one can achieve well defined outputs.

In figure 26 the monolithic structure studied and the corresponding external set-up are shown. V_x and V_y are applied to the left and the right branch of YBS1. The stem of YBS1, due to the monolithic integration, simultaneously acts as the left side gate of YBS2. YBS2 functions as a differential amplifier. An external feedback is introduced by feeding back the left branch output voltage to the right side gate. As external resistances, $R_{bl} = R_{br} = 10\,M\Omega$ are used and the bias voltage is set to 1.0 V. For an efficient cascading of electronic devices it is important that the logic H level (L level) of the output stage fits to the input stage of the next cascaded junction.

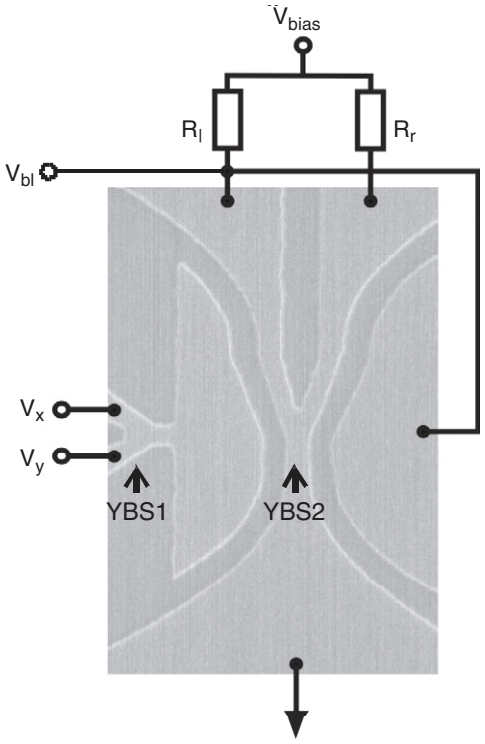

Figure 26. Scanning electron microscope image of an integrated monolithic AND/NAND gate with a width of the current conducting channels of about 100 nm.

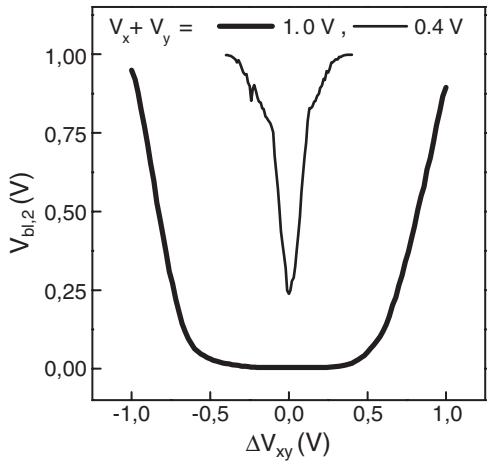

Figure 27. Voltage $V_{\mathrm{bl},2}$ at the NAND output of an integrated AND/NAND gate as a function of the voltage difference ΔV_{xy} between the inputs. The input voltages are varied in push–pull configuration without an external feedback coupling for two working point settings $V_x + V_y = 0.4$ V (thin line) and $V_x + V_y = 1.0$ V (thick line).

First the ballistic feedback of the integrated AND/NAND layout was investigated without the use of any external feedback ($V_{\mathrm{gr}} \neq V_{\mathrm{bl}}$). For this purpose V_{bl} was detected in a push–pull varied mode of the inputs for a variation of ΔV_{xy} with $V_x + V_y = 0.4$ V and for $V_x + V_y = 1.0$ V (figure 27). In both cases a pronounced minimum occurs at the output branch of YBS2 for $\Delta V_{xy} = 0$. The sum of the input voltages defines the working point of the YBS which affects the position and the shape of the $V_{\mathrm{bl},2}(\Delta V_{xy})$ curve. In particular, the maximum conductance $G_{\mathrm{sl,max}}$ and the value of the voltage minimum $V_{\mathrm{bl,min}} = V_{\mathrm{bias}}(1 + RG_{\mathrm{sl,max}})^{-1}$, respectively, are determined by the sum $V_x + V_y$ at $\Delta V_{xy} = 0$.

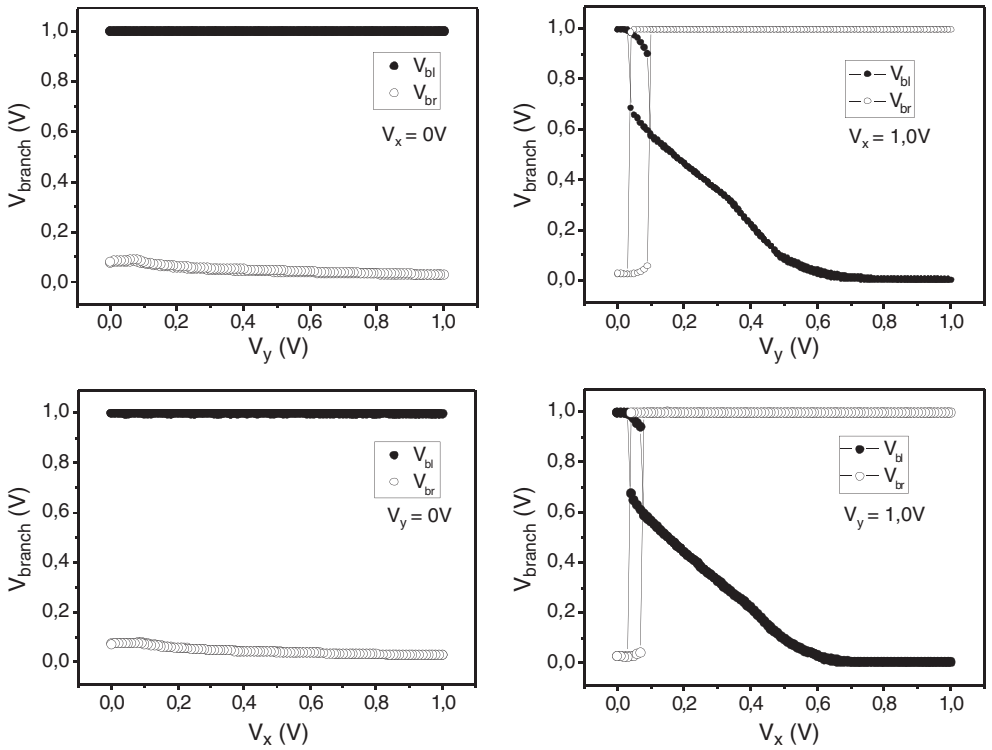

Figure 28. Experimentally studied transfer characteristics of the monolithic YBS AND/NAND gate with an external feedback coupling. For each characteristic one input voltage (V_x or V_y) was kept constant (0 or 1 V) and the other one was swept up and down between 0 and 1 V.

For the coupled YBSs investigated a working point defined by $V_x + V_y = 0.4$ V turns out to be too low in view of the output voltage swing, whereas an increase of $V_x + V_y$ to 1.0 V nicely meets the conditions for the realization of the AND/NAND gate. Starting from a symmetrical gate drive ($\Delta V_{xy} = 0$, $V_{\mathrm{bl,min}} = 33$ mV) the output voltage $V_{\mathrm{bl},2}$ first increases moderately for positive as well as for negative voltage differences ΔV_{xy} and then more intensely for $|\Delta V_{xy}| > 0.5$ V. It reaches almost the applied bias voltage for $|\Delta V_{xy}| \approx 1.0$ V. The symmetrical $V_{\mathrm{bl},2}(\Delta V_{xy})$ characteristic with respect to $\Delta V_{xy} = 0$ is ascribed to ballistic rectification in the Y-shaped input junction. As a result, it follows that the left side gate $V_{\mathrm{gl}} < (1/2)(V_x + V_y)$; thus $|\Delta V_{xy}| > 0$. On the basis of the symmetrical circuit with $\Delta V_{xy} = 0$ the voltage at the left side gate of the YBS2 and therefore the conductance G_{sl} decrease with increasing ΔV_{xy} leading to the observed rising of $V_{\mathrm{bl},2}$ with increasing difference of the input voltages.

With an external feedback one obtains the transfer characteristic presented in figure 28. In each of the four corresponding characteristics, one input is set to H for $V_{x,y} > 0.9$ V or to L for $V_{x,y} < 0.1$ V, while the second input is swept up from 0 to 1.0 V and then back to 0. In the top left transfer characteristics ($V_x = 0$) as well as and bottom left ($V_y = 0$) transfer characteristic, one input is kept at a high electrochemical potential. Due to the ballistic rectification effect in YBS1 the stem voltage is only weakly changed by the voltage sweep. Hence no state transition occurs for $V_{\mathrm{bl,br}}$. For the characteristics (top left and bottom right) the input voltage V_x is kept at an H level. At the beginning of the voltage sweep V_{br} is set to L and V_{bl} to H. On increasing V_y the increase of the voltage drop at the stem of YBS1 enhances the conductance

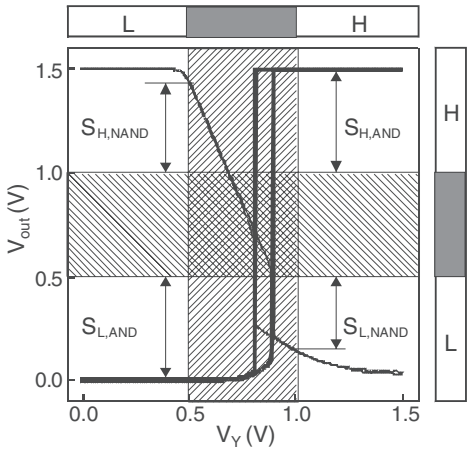

Figure 29. Level definition of a combined AND/NAND gate. The output signals $V_{bl,2}$ (thin line, NAND output) and $V_{br,2}$ (thick line, AND output) are shown as a function of V_y for $V_x = 1.5$ V. The forbidden, non-defined regions of the input and output voltage, respectively, are hatched.

between the left branch and the stem of YBS2. The internal and external feedback couplings trigger a bistable transition for V_{bl} from L to H and also one from H to L in the V_{br} curve when the threshold voltage $V_{L\to H} = 0.09$ V is reached. Finally, during the down-sweep the initial state configuration, $V_{bl} = H$ and $V_{br} = L$, is restored for $V_y = V_{H\to L} = 0.04$ V. The hysteretic width is about 60 mV. An analogous explanation can be advanced for the transfer characteristic shown in the bottom right graph which is almost identical to the above-described case except that V_x is exchanged with V_y. Small differences in the hysteresis ($V_{Hys} = 40$ mV) are associated with unintended asymmetries of the device.

In digital systems logic gates are combined together to a greater or lesser extent forming complex circuits. The output of one stage is then driving the inputs of several subsequent logic gates. That means, consequently, that the inputs of the connect gates with finite input resistances represent loads and thus they affect the height of the control output of the previous gate. As a result in both switching states (L, H) the switching voltage at the output is different compared to the case when no load exists at all. In addition, fluctuations of the bias voltage, heating and crosstalk between adjacent signal wires may degrade the output level of a logic gate. Therefore, for logic gates certain voltage margins are defined rather then discrete threshold voltages in order to define logic H and L levels. In figure 29 we have defined such logic margins for the AND (thin line) and the NAND (thick line) output. The hatched areas give a possible definition of the logic levels. Voltages in the interval [1.0, 1.5 V] ([0, 0.5 V]) are associated with the binary signal level H (L), while voltages in the interval]0.5 V, 1.0 V[are associated with the forbidden, non-defined region.

From this definition the static noise margin S is extracted (figure 30). Due to the Schmitt trigger characteristic, which is particularly noticeable for the transfer curve of the AND output as a strong nonlinear dependence, the absolute noise margin for both signal levels is about 0.5 V and relative one is 0.33 (related to the bias voltage $V_{cc} = V_{bias} = 1.5$ V).

The rectifying features of the input junction in combination with the inverting behaviour of $V_{bl,2}$, due to a variation of V_{gl}, lead to an output voltage $V_{bl,2}$ which fulfils the X NAND Y functionality. An external feedback of the output voltage $V_{bl,2}$ to the right side gate of the YBS results in a bistable switching with the advantage of a large noise margin and well defined output levels $\overline{C} = X$ NAND Y and $C = X$ NAND Y at the left and right branches of

	S_{AND} [mV]	s_{AND}	S_{NAND} [mV]	s_{NAND}
H	500	0.33	431	0.29
L	500	0.33	360	0.29

Figure 30. Comparison of the static noise margins of a combined AND/NAND gate. The table presents the absolute (S) as well as the relative noise margin $s = S/V_{cc}$ for a bias voltage of $V_{cc} = 1.5$ V for the YBS AND/NAND logic.

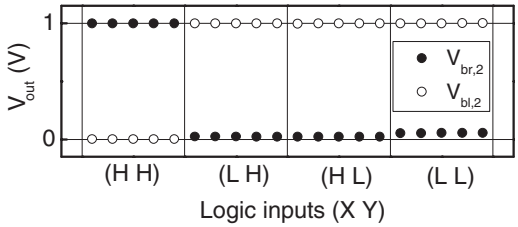

Figure 31. Depiction of the logic functionality for an integrated AND/NAND gate. The output signals $V_{bl,2}$ and $V_{br,2}$ are sketched, depending on all combinations of the logic input levels for X and Y. The input stage X, Y is set to an H (L) state for $V_{x,y} = 1.0$ V ($V_{x,y} = 0$).

the YBS. The resulting voltages ($V_{bl,2}$ and $V_{br,2}$) are shown in figure 31 as a function of all possible combinations of the logic input levels, where the input signal is H (L) for $V_{x,y} = 1.0$ V ($V_{x,y} = 0$). It is obvious, that the integrated AND/NAND gate fulfils the corresponding truth.

6. Summary

In this review, we have shown how quantum wires and Y-branches based on modulation doped GaAs/AlGaAs heterostructures may be used for nanoelectronic applications exploiting ballistic transport. Transport spectroscopy of wet etched quantum wires reveals subband spacings exceeding 20 meV. In addition, signatures of ballistic transport are found in the transconductance characteristic. Quantum wires have been exploited as amplifiers. In nanoelectronic Y-branches with dimensions much smaller than the electron mean free path, bias voltage variations applied between two branches result in a rectified voltage output at the central stem. This ballistic rectification effect was reviewed as a basis for several logic gates. Recent studies of a capacitive coupling of Y-branch switches leading to an additional amplification were discussed. This together with suitable local feedback circuits results in bistable switching behaviours. In summary, the ballistic rectification as well as the self-gating mechanism provide new functions of these nanoelectronic switches observable only in the nonlinear transport regime.

Acknowledgments

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